Taming Delays in Cyber-Physical Systems

Towards a Theory of Networked Hybrid Systems

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HTD-Tutorial · Houston · December 2020



Motivation ••••••••• Concluding Remarks

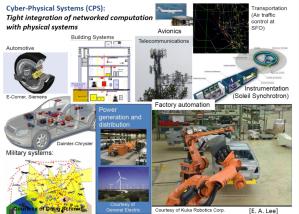
Cyber-Physical Systems

"The term cyber-physical systems (CPS) refers to a new generation of systems with integrated computational and physical capabilities that can interact with humans through many new modalities. The ability to interact with, and expand the capabilities of, the physical world through computation, communication, and control is a key enabler for future technology developments."

[Radhakisan Baheti and Helen Gill, The Impact of Control Technology, 2011]

Cyber-Physical Systems

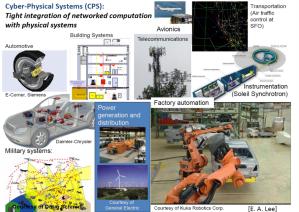
An open, interconnected form of embedded systems, among which many are safety-critical.



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Cyber-Physical Systems

An open, interconnected form of embedded systems, among which many are safety-critical.



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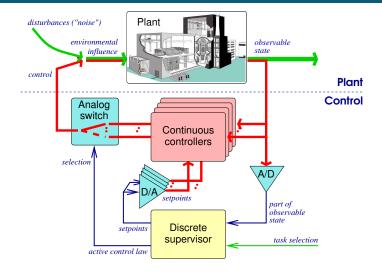
"How can we provide people with CPS they can bet their lives on?"

[Jeannette Wing]

Motivation
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Formal Verification ୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦୦ Concluding Remarks

Hybrid Systems

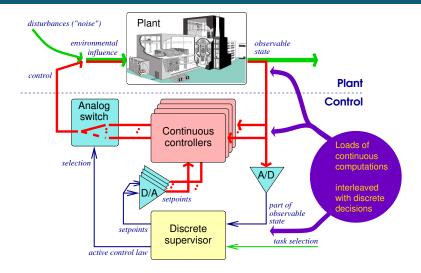


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Formal Verification

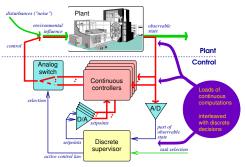
Concluding Remarks

Hybrid Systems



Formal Verification

Hybrid Systems



Crucial question :

How do the controller and the plant interact?

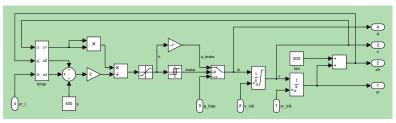
Traditional answer:

- Coupling assumed to be (or at least modelled as) delay-free.
- ⇒ Mode dynamics is covered by the conjunction of the individual ODEs.
- Switching btw. modes is an immediate reaction to environmental conditions.

Motivation	Con
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Concluding Remarks

Instantaneous Coupling



©ETCS-3

Following the tradition, above (rather typical) Simulink model assumes

- delay-free coupling between all components,
- instantaneous feed-through within all functional blocks.

Central questions :

- Is this realistic?
- If not, does it have observable effect on control performance?
- May that effect be detrimental or even harmful?

Controller Synthesis

Formal Verification

Concluding Remarks

Q1: Is Instantaneous Coupling Realistic?



Digital control needs A/D and D/A conversion, which induces latency in signal forwarding.



Digital signal processing, especially in complex sensors like CV, needs processing time, adding signal delays.



Networked control introduces communication latency into the feedback control loop.



Harvesting, fusing, and forwarding data through sensor networks enlarge the latter by orders of magnitude.

Controller Synthesis

Concluding Remarks

Q1 : Is Instantaneous Coupling Realistic? – No.



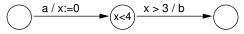


Harvesting, fusing, and forwarding data through sensor networks enlarge the latter by orders of magnitude.

Q1a : Resultant Forms of Delay

Delayed reaction : Reaction to a stimulus is not immediate.

Easy to model in timed automata, hybrid automata, etc. :

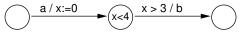


- Thus amenable to the pertinent analysis tools.
- ⇒ Not of interest today.

Q1a : Resultant Forms of Delay

Delayed reaction : Reaction to a stimulus is not immediate.

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Network delay : Information of different age coexists and is queuing in the network when piped towards target.

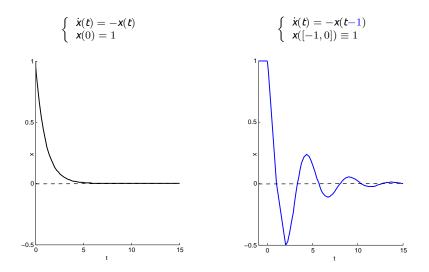
- End-to-end latency may exceed sampling intervals etc. by orders of magnitude
- Not (continuous-time pipelined delay) or not efficiently (discrete-time pipelined delay) expressible in our std. models.
- ⇒ Our theme today.

Controller Synthesis

Formal Verification

Concluding Remarks

Q2 : Do Delays Have Observable Effect?



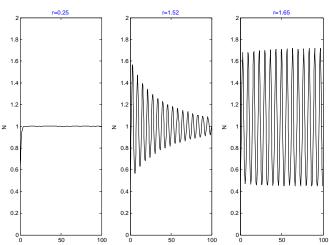
Controller Synthesis

Formal Verification

Concluding Remarks

Q2 : Do Delays Have Observable Effect?

Delayed logistic equation [G. Hutchinson, 1948]:



 $\dot{N}(t) = N(t)[1 - N(t - r)]$

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Controller Synthesis

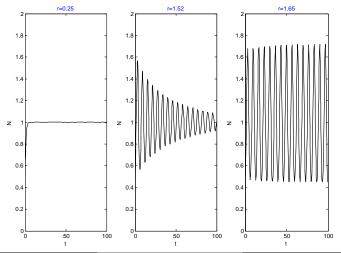
Formal Verification

Concluding Remarks

Q2 : Do Delays Have Observable Effect? - Yes, they have.

Delayed logistic equation [G. Hutchinson, 1948]:

$$N(t) = N(t)[1 - N(t - r)]$$



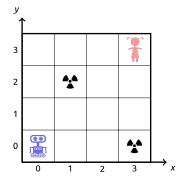
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Controller Synthesis

Formal Verification

Concluding Remarks

Q3 : May the Effects be Harmful?



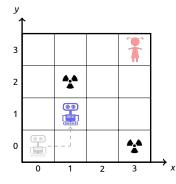
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Controller Synthesis

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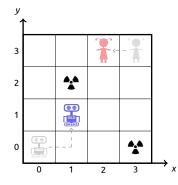
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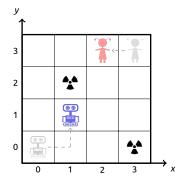
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Controller Synthesis

Formal Verification

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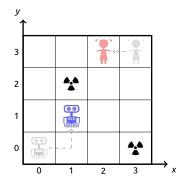
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Formal Verification

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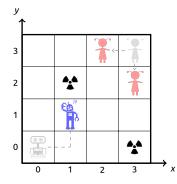
No delay :

Robot always wins by circling around the obstacle at (1,2).

Formal Verification

Concluding Remarks

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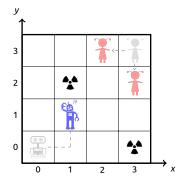
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1 step delay :

Formal Verification

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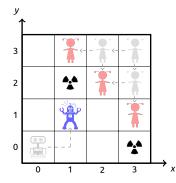
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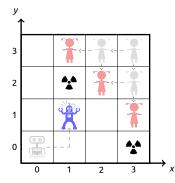
1 step delay :

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2 steps delay :

Concluding Remarks

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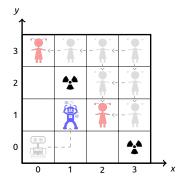
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2 steps delay :

Robot still wins, yet extra memory is needed.

Concluding Remarks

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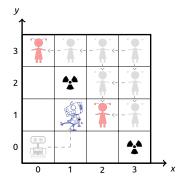
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3 steps delay :

Concluding Remarks

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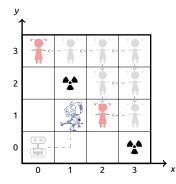
3 steps delay :

Robot is unwinnable (uncontrollable) anymore.

Controller Synthesis

Formal Verification

Q3 : May the Effects be Harmful? – Yes, delays may well annihilate control performance.



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Motivation	Controller Synthesis	Formal Verification	Concluding Remarks
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Consequences

- Delays in feedback control loops are ubiquitous.
- They may well invalidate the safety/stability/...certificates obtained by verifying delay-free abstractions of the feedback control systems.

Automatic verification/synthesis methods addressing feedback delays in hybrid systems should therefore abound!

Consequences

- Delays in feedback control loops are ubiquitous.
- They may well invalidate the safety/stability/...certificates obtained by verifying delay-free abstractions of the feedback control systems.

Automatic verification/synthesis methods addressing feedback delays in hybrid systems should therefore abound ! Surprisingly, they don't :

M. Peet. S. Lall : Constructing Lyponov functions for nonlinear DDEs using SDP (NOLCOS '04)

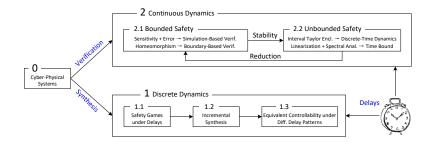
- 2 S. Prajna, A. Jadbabaie : Meth. f. safety verification of time-delay syst. (CDC '05)
- 3 L. Zou, M. Fränzle, N. Zhan, P. N. Mosaad : Autom. verific. of stabil. and safety (CAV '15)
- 4 H. Trinh, P. T. Nam, P. N. Pathirana, H. P. Le : On bwd.s and fwd.s reachable sets bounding for perturbed time-delay systems (Appl. Math. & Comput. 269, '15)
- S Z. Huang, C. Fan, S. Mitra : Bounded invariant verif. for time-delayed nonlinear networked dyn. syst. (NAHS '16)
- 6 P. N. Mosaad, M. Fränzle, B. Xue : Temporal logic verification for DDEs (ICTAC '16)
- 7 M. Chen, M. Fränzle, Y. Li, P. N. Mosaad, N. Zhan : Validat. simul.-based verific. (FM '16)
- 3 B. Xue, P. N. Mosaad, M. Fränzle, M. Chen, Y. Li, N. Zhan : Safe approx. of reach. sets for DDEs (FORMATS '17)
- 9 E. Goubault, S. Putot, L. Sahlman : Approximating flowpipes for DDEs (CAV'18)
- 🔟 M. Chen, M. Fränzle, Y. Li, P. N. Mosaad, N. Zhan : Synthesiz. controllers resilient to delayed interact. (ATVA '18)
- 🔟 S. Feng, M. Chen, N. Zhan, M. Fränzle, B. Xue : Taming delays in dyn. syst. : Unbounded verif. of DDEs (CAV '19)
- [M. Zimmermann. LICS '18, GandALF '17], [F. Klein & M. Zimmermann. ICALP '15, CSL '15]

(plus a handful of related versions)

Formal Verification

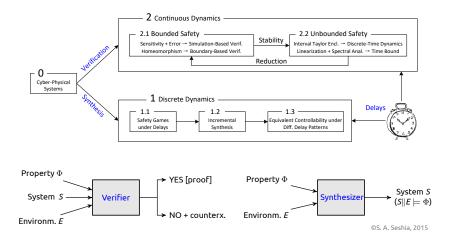
Concluding Remarks

Overview of the Tutorial



Formal Verification

Overview of the Tutorial



ormal Verification

Concluding Remarks

The Agenda



Outline

1 Synthesizing Safe Controllers Resilient to Delayed Interaction

- Safety Games under Delays
- Incremental Synthesis
- Equivalent Controllability

2 Verifying Safety of Delayed Differential Dynamics

- Delayed Differential Dynamics
- Bounded Safety Verification
- Unbounded Safety Verification

3 Concluding Remarks

Summary

Solving Discrete Safety Games

Staying safe and reaching an objective when observation & actuation are confined by delays

—Joint work with M. Fränzle, Y. Li, and P. N. Mosaad—



Controller Synthesis

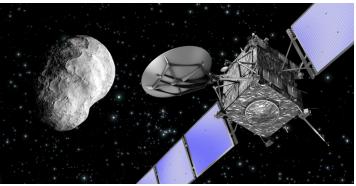
ormal Verification

Concluding Remarks

Delayed Safety Games

Staying Safe

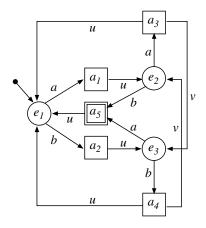
When Observation & Actuation Suffer from Serious Delays



©ESA

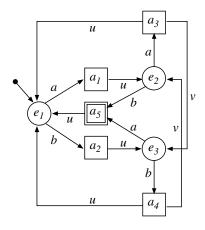
- You could move slowly. (Well, can you?)
- You could trust autonomy.
- Or you have to anticipate and issue actions early.

Motivation 0000000000	Controller Synthesis	Formal Verification	Concluding Remarks		
Delayed Safety Games					
Δ Trivial Safety Game					



Goal: Avoid a_5 by appropriate actions of player *e*.

Motivation	Controller Synthesis	Formal Verification	Concluding Remarks
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Delayed Safety Games			
Δ Trivial Saf	etv Game		



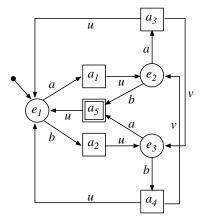
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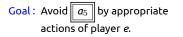
Strategy: May always play "*a*" except in *e*₃:

$$e_1, e_2 \mapsto a$$

 $e_3 \mapsto b$

Motivation	Controller Synthesis	Formal Verification	Concluding Remarks
Delayed Safety Games			
A Trivial Safe	etv Game		





Strategy: May always play "*a*" except in *e*₃:

 $egin{aligned} \mathbf{e}_1, \mathbf{e}_2 &\mapsto \mathbf{a} \ \mathbf{e}_3 &\mapsto \mathbf{b} \end{aligned}$

Properties : Determinacy and memoryless.

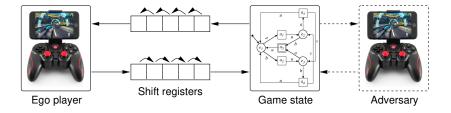
Controller Synthesis

Formal Verification

Concluding Remarks

Delayed Safety Games

Playing Safety Game Subject to Discrete Delay



Observation : It doesn't make an observable difference for the joint dynamics whether delay occurs in perception, actuation, or both.

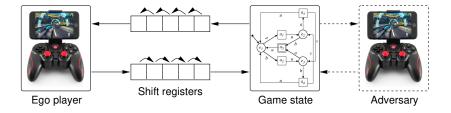
Controller Synthesis

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Delayed Safety Games

Playing Safety Game Subject to Discrete Delay



Observation : It doesn't make an observable difference for the joint dynamics whether delay occurs in perception, actuation, or both. Consequence : There is an¹obvious reduction to a safety game of perfect information.

^{1.} In fact, two different ones: To mimic opacity of the shift registers, delay has to be moved to actuation/sensing for ego/adversary, resp. The two thus play different games!

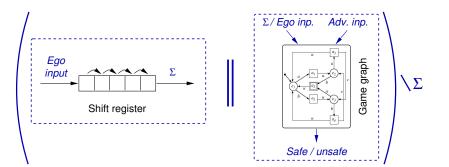
Controller Synthesis

Concluding Remarks

Delayed Safety Games

Reduction to Delay-Free Games

from Ego-Player Perspective

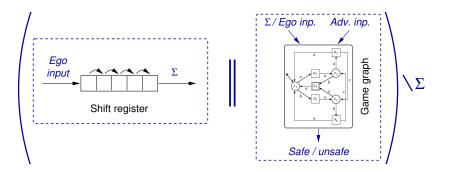


Concluding Remarks

Delayed Safety Games

Reduction to Delay-Free Games

from Ego-Player Perspective



- © Safety games w. delay can be solved algorithmically.
- © Game graph incurs blow-up by factor |Alphabet(ego)|^{delay}.

Controller Synthesis

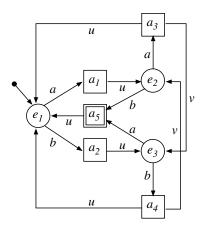
Formal Verification

Concluding Remarks

Delayed Safety Games

The Simple Safety Game

...but with Delay



No delay :

$$egin{array}{ccc} egin{array}{ccc} eta_1, eta_2 \mapsto eta & eba & eb$$

1 step delay : Strategy? $a_1, a_4 \mapsto a$ $a_2, a_3 \mapsto b$

Controller Synthesis

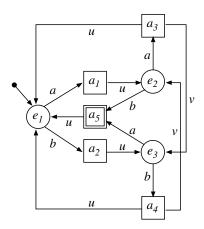
Formal Verification

Concluding Remarks

Delayed Safety Games

The Simple Safety Game

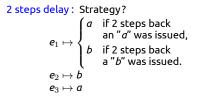
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Need memory!

Controller Synthesis

Formal Verification

Concluding Remarks

Incremental Synthesis

Incremental Synthesis in a Nutshell

Observation : A winning strategy for delay k' > k can always be utilized for a safe win under delay k.

Consequence : A position is winning for delay *k* is a necessary condition for it being winning under delay *k'* > *k*.

M. Chen, M. Fränzle, Y. Li, P. N. Mosaad, N. Zhan : What's to come is still unsure : Synthesizing controllers resilient to delayed interaction. ATVA '18. [Distinguished Paper Award].

Controller Synthesis

Formal Verification

Concluding Remarks

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Incremental Synthesis in a Nutshell

Observation : A winning strategy for delay k' > k can always be utilized for a safe win under delay k.

Consequence : A position is winning for delay k is a necessary condition for it being winning under delay k' > k.

- Idea : Incrementally filter out loss states & incrementally synthesize winning strategy for the remaining :
 - Synthesize winning strategy for the delay-free counterpart;
 - **2** For each winning state, lift strategy from delay k to k + 1;
 - Remove states where this does not succeed;
 - Repeat from 2 until either delay-resilience suffices (winning) or initial state turns lossy (losing).
- M. Chen, M. Fränzle, Y. Li, P. N. Mosaad, N. Zhan : What's to come is still unsure : Synthesizing controllers resilient to delayed interaction. ATVA '18. [Distinguished Paper Award].

Controller Synthesis

Formal Verification

Concluding Remarks

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Incremental Synthesis

Incremental Synthesis of Delay-Tolerant Strategies

1 Generate a *maximally permissive* strategy for delay k = 0.

Controller Synthesis

Concluding Remarks

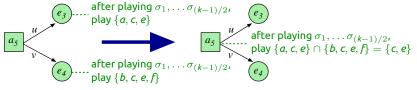
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Incremental Synthesis

Incremental Synthesis of Delay-Tolerant Strategies

- **1** Generate a *maximally permissive* strategy for delay k = 0.
- 2 Advance to delay k + 1:

If k odd : For each (ego-)winning adversarial state define strategy as



... and eliminate any dead ends by bwd. traversal.

Controller Synthesis

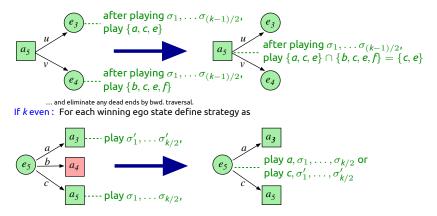
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Incremental Synthesis

Incremental Synthesis of Delay-Tolerant Strategies

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Controller Synthesis

Formal Verification

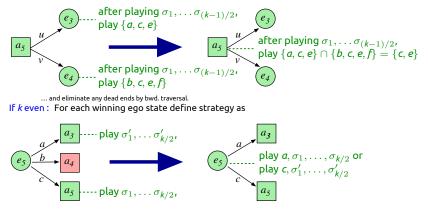
Concluding Remarks

Incremental Synthesis

Incremental Synthesis of Delay-Tolerant Strategies

- **1** Generate a maximally permissive strategy for delay k = 0.
- 2 Advance to delay k + 1:

If k odd : For each (ego-)winning adversarial state define strategy as



3 Repeat from 2 until either delay-resilience suffices or initial state turns lossy.

Controller Synthesis

Formal Verification

Concluding Remarks

Incremental Synthesis

Incremental vs. Reduction-Based

Ben	chmai	'n		Reduction + Explicit-State Synthesis					5	Incremental Explicit-State Synthesis						
name	S	$ \rightarrow $	$ \mathcal{U} $	δ_{\max}	$\delta = 0$	$\delta = 1$	$\delta = 2$	$\delta = 3$	$\delta = 4$	δ_{\max}	$\delta = 0$	$\delta = 1$	$\delta = 2$	$\delta = 3$	$\delta = 4$	%
Exmp.trv1	14	20	4	> 22	0.00	0.00	0.01	0.02	0.02	> 30	0.00	0.00	0.00	0.01	0.01	
Exmp.trv2	14	22	4	= 2	0.00	0.01	0.01	0.02	-	= 2	0.00	0.00	0.00	0.01	_	81.97
Escp.4×4	224	738	16	= 2	0.08	11.66	11.73	1059.23	_	= 2	0.08	0.13	0.22	0.25	-	99.02
Escp.4×5	360	1326	20	= 2	0.18	34.09	33.80	3084.58	-	= 2	0.18	0.27	0.46	0.63	-	99.02
Escp.5×5	598	2301	26	> 2	0.46	96.24	97.10	?	?	= 2	0.46	0.68	1.16	1.71	-	98.98
Escp.5×6	840	3516	30	≥ 2	1.01	217.63	216.83	?	?	= 2	1.00	1.42	2.40	4.30	-	99.00
Escp.6×6	1224	5424	36	≥ 2	2.13	516.92	511.41	?	?	= 2	2.06	2.90	5.12	10.30	-	98.97
Escp.7x7	2350	11097	50	≥ 2	7.81	2167.86	2183.01	?	?	= 2	7.71	10.67	19.04	52.47	_	98.99
Escp.7×8	3024	14820	56	≥ 0	13.07	?	?	?	?	= 2	13.44	18.25	32.69	108.60	-	99.01
Benchmar	Benchmark Reduction + Yosys + SafetySynth (symbolic) Incre						cremental	Synthe	esis (exp	olicit-sta	ate imple	mentati	ion)			
name	δ_{max}	$\delta = 0$	δ =	$= 1 \delta =$	$2 \delta =$	$3 \delta = 4$	$\delta =$	$5 \delta = 6$	$\delta = 0$	$\delta = 1$	$\delta = 2$	$\delta = 3$	$\delta = 4$	$\delta = 5$	$\delta = 6$	%
Stub.4×4	= 2	1.07	/ 1.	.24 1.	24 1.	80 -			0.04	0.07	0.12	0.18	-	-	-	98.98
Stub.4×5	= 2	1.16	5 1.	.49 1.	49 2.	83 -			0.08	0.14	0.25	0.44	-	-	-	98.97
Stub.5×5	= 2	1.19	2	.61 2.	50 13.	67 -			0.21	0.37	0.63	1.17	-	-	-	98.97
Stub.5×6	= 2	1.18	3 2.	.60 2.	59 23.	30 -			0.42	0.69	1.20	2.49	-	-	_	98.96
Stub.6×6	= 4	1.17	2	.76 2.	74 19.	96 19.69	655.2	4 –	0.93	1.47	2.60	5.79	7.54	7.60	_	99.89
Stub.7×7	= 4	1.23	3 2.	.50 2.	48 24.	57 23.01	2224.6	2 –	3.60	5.52	10.08	22.75	31.18	32.98	-	99.88

Table - Benchmark results in relation to reduction-based approaches (time in seconds)

Controller Synthesis

Formal Verification

Concluding Remarks

Incremental Synthesis

Incremental vs. Reduction-Based

Ben	chmar	k	Reduction + Explicit-State Synthesis					5	Incremental Explicit-State Synthesis							
name	S	$ \rightarrow $	$ \mathcal{U} $	δ_{\max}	$\delta = 0$	$\delta = 1$	$\delta = 2$	$\delta = 3$	$\delta = 4$	$\delta_{\rm max}$	$\delta = 0$	$\delta = 1$	$\delta = 2$	$\delta = 3$	$\delta = 4$	%
Exmp.trv1	14	20	4	≥ 22	0.00	0.00	0.01	0.02	0.02	≥ 30	0.00	0.00	0.00	0.01	0.01	
Exmp.trv2	14	22	4	= 2	0.00	0.01	0.01	0.02	-	= 2	0.00	0.00	0.00	0.01	-	81.97
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Benchman	Benchmark Reduction + Yosys + SafetySynth (symbolic) Incremental Synthesis (explicit-state implementation)							on)								
name	δ_{max}	$\delta = 0$	$\delta =$	$1 \delta =$	$2 \delta =$	$3 \delta = 4$	$\delta = \delta$	$5 \delta = 6$	$\delta = 0$	$\delta = 1$	$\delta = 2$	$\delta = 3$	$\delta = 4$	$\delta = 5$	$\delta = 6$	%
Stub.4×4	= 2	1.07	71.	24 1.	24 1.	80 -			0.04	0.07	0.12	0.18	-	-	-	98.98
Stub.4×5	= 2	1.16	51.	49 1.	49 2.	83 -			0.08	0.14	0.25	0.44	-	-	_	98.97
Stub.5×5	= 2	1.19	2.	61 2.	50 13.	67 -			0.21	0.37	0.63	1.17	-	-	_	98.97
Stub.5×6	= 2	1.18	3 2.	60 2.	59 23.	30 -			0.42	0.69	1.20	2.49	-	-	_	98.96
Stub.6×6	= 4	1.17	7 2.	76 2.	74 19.	96 19.69	655.2	4 –	0.93	1.47	2.60	5.79	7.54	7.60	_	99.89
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Table - Benchmark results in relation to reduction-based approaches (time in seconds)

Controller Synthesis

Formal Verification

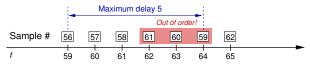
Concluding Remarks

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Equivalent Controllability

How about Non-Order-Preserving Delays?

Observations may arrive out-of-order :



Controller Synthesis

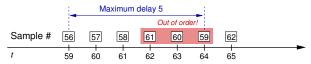
Formal Verification

Concluding Remarks

Equivalent Controllability

How about Non-Order-Preserving Delays?

Observations may arrive out-of-order :



© But this may only reduce effective delay, improving controllability :



Controller Synthesis

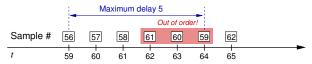
Formal Verification

Concluding Remarks

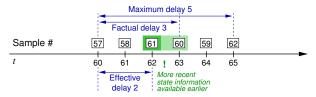
Equivalent Controllability

How about Non-Order-Preserving Delays?

Observations may arrive out-of-order :



But this may only reduce effective delay, improving controllability :



- W.r.t. qualitative controllability, the worst-case of out-of-order delivery is equivalent to order-preserving delay k.
- © Stochastically expected controllability even better than for strict delay *k*.

Controller Synthesis

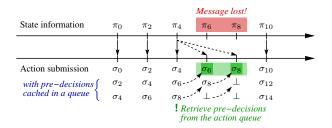
Formal Verification

Concluding Remarks

Equivalent Controllability

How About (Bounded) Message Loss?

© Message carrying the state information may get lost :



The controller can still win a safety game in the presence of bounded message loss leveraging delay-resilient strategies.

Controller Synthesis

Concluding Remarks

Equivalent Controllability

Equivalence of Qualitative Controllability

Theorem (Equivalence of qualitative controllability)

Given a two-player safety game, the following statements are equivalent if δ is even :

- **There exists a winning strategy under an exact delay of** δ , i.e., if at any point of time t the control strategy is computed based on a prefix of the game that has length $t \delta$.
- **2** There exists a winning strategy under time-stamped out-of-order delivery with a maximum delay of δ , i.e., if at any point of time t the control strategy is computed based on the complete prefix of the game of length $t \delta$ plus potentially available partial knowledge of the game states between $t \delta$ and t.
- **There exists a winning strategy when at any time t = 2n, i.e., any player-0 move, information on the game state at some time t' \in \{t 2k, ..., t\} is available, i.e., under out-of-order delivery of messages with a maximum delay of \delta and a maximum number of consecutively lost upstream or downstream messages of \frac{\delta}{2}.**

The first two equivalences do also hold for odd δ .

M. Chen, M. Fränzle, Y. Li, P. N. Mosaad, N. Zhan : Indecision and delays are the parents of failure : Taming them algorithmically by synthesizing delay-resilient control. Acta Informatica '20.

Outline

1 Synthesizing Safe Controllers Resilient to Delayed Interaction

- Safety Games under Delays
- Incremental Synthesis
- Equivalent Controllability

2 Verifying Safety of Delayed Differential Dynamics

- Delayed Differential Dynamics
- Bounded Safety Verification
- Unbounded Safety Verification

3 Concluding Remarks

Summary

Solving Delay Differential Equations (DDEs)

A formal model of delayed feedback control

—Joint work with M. Fränzle, Y. Li, S. Feng, P. N. Mosaad, B. Xue, and L. Zou—



Controller Synthesis

Formal Verification

Concluding Remarks

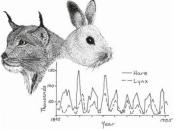
Delayed Differential Dynamics

Delayed Coupling in Differential Dynamics



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Predator-prey dynamics

Controller Synthesis

Formal Verification

Concluding Remarks

Delayed Differential Dynamics

Delayed Coupling in Differential Dynamics



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Predator-prey dynamics

"Despite [...] very satisfactory state of affairs as far as [ordinary] differential equations are concerned, we are nevertheless forced to turn to the study of more complex equations. Detailed studies of the real world impel us, albeit reluctantly, to take account of the fact that the rate of change of physical systems depends not only on their present state, but also on their past history."

[Richard Bellman and Kenneth L. Cooke, 1963]

193.5

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Controller Synthesis

Formal Verification

Concluding Remarks

Delayed Differential Dynamics

Delay Differential Equations (DDEs)

$$\begin{cases} \dot{\mathbf{x}}(t) = \boldsymbol{f}(\mathbf{x}(t), \mathbf{x}(t-r_1), \dots, \mathbf{x}(t-r_k)), \quad t \in [0, \infty) \\ \mathbf{x}(t) = \boldsymbol{\phi}(t), \quad t \in [-r_{\max}, 0] \end{cases}$$

Controller Synthesis

Formal Verification

Concluding Remarks

Delayed Differential Dynamics

Delay Differential Equations (DDEs)

$$\begin{cases} \dot{\mathbf{x}}(t) = \boldsymbol{f}(\mathbf{x}(t), \mathbf{x}(t-r_1), \dots, \mathbf{x}(t-r_k)), \quad t \in [0, \infty) \\ \mathbf{x}(t) = \boldsymbol{\phi}(t), \quad t \in [-r_{\max}, 0] \end{cases}$$

Controller Synthesis

Formal Verification

Concluding Remarks

Delayed Differential Dynamics

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The unique *solution* (*trajectory*): $\xi_{\phi}(t)$: $[-r_{\max}, \infty) \mapsto \mathbb{R}^{n}$.

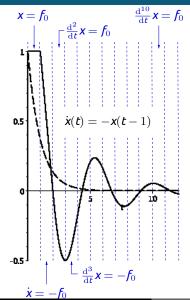
Controller Synthesis

Formal Verification

Concluding Remarks

Delayed Differential Dynamics

Why DDEs are Hard(er)



DDEs constitute a model of system dynamics beyond "state snapshots" :

- They feature "functional state" instead of state in the ℝⁿ.
- Thus providing rather infallible, infinite-dimensional memory of the past.

N.B. : More complex transformations may be applied to the initial segment f_0 according to the DDE's right-hand side. f_0 will nevertheless hardly ever vanish from the state space.

N. Zhan · ISCAS&CCF-TCFM, M. Chen · RWTH Aachen

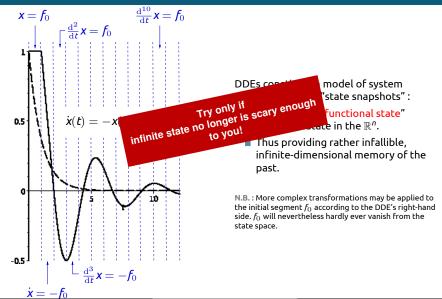
Controller Synthesis

Formal Verification

Concluding Remarks

Delayed Differential Dynamics

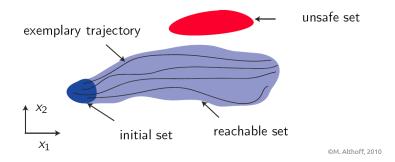
Why DDEs are Hard(er)



N. Zhan · ISCAS&CCF-TCFM, M. Chen · RWTH Aachen Tan

Motivation 0000000000	Controller Synthesis	Formal Verification	Concluding Remarks
Delayed Differential Dyn	amics		
Safety Veri	fication Problem		
Given T∈	\mathbb{R} . $\mathcal{X}_0 \subset \mathbb{R}^n$. $\mathcal{U} \subset \mathbb{R}^n$. we	eather	

$$\forall \boldsymbol{\phi} \in \{\boldsymbol{\phi} \mid \boldsymbol{\phi}(\boldsymbol{t}) \in \mathcal{X}_0, \forall \boldsymbol{t} \in [-\boldsymbol{r}_{\max}, 0]\}: \quad \left(\bigcup_{\boldsymbol{t} \leq \boldsymbol{\mathcal{T}}} \boldsymbol{\xi}_{\boldsymbol{x}_0}(\boldsymbol{t})\right) \cap \mathcal{U} = \emptyset \quad ?$$



System is *T*-safe, if no trajectory enters \mathcal{U} within $[-r_{\max}, T]$; Unbounded : ∞ -safe.

Bounded Verification

Bounded Safety Verification of DDEs



Controller Synthesis

Formal Verification

Concluding Remarks

Bounded Verification – Validated Simulation-Based

Simulation-Based Verification Framework

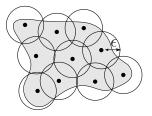


Figure – A finite ϵ -cover of the initial set of states.

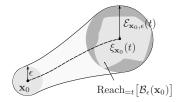


Figure – An Over-approximation of the reachable set by bloating the simulation.

©A. Donzé & O. Maler, 2007

Controller Synthesis

Formal Verification

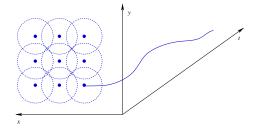
Concluding Remarks

Bounded Verification – Validated Simulation-Based

Validated Simulation-Based Verification

Do numerical simulation on a (sufficiently dense) sample of initial states.

- Z Add (pessimistic) local-error by solving an optimization problem.
- **B** "Bloat" the resulting trajectories by sensitivity analysis.



⇒ M. Chen, M. Fränzle, Y. Li, P. N. Mosaad, N. Zhan : Validat. simul.-based verific.. FM'16.

Controller Synthesis

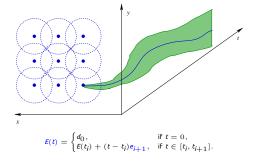
Formal Verification

Concluding Remarks

Bounded Verification – Validated Simulation-Based

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Controller Synthesis

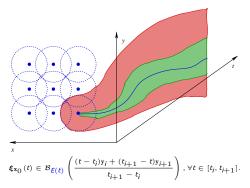
Formal Verification

Concluding Remarks

Bounded Verification – Validated Simulation-Based

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Controller Synthesis

Formal Verification

Concluding Remarks

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Bounded Verification – Validated Simulation-Based

Example : Delayed Logistic Equation

[G. Hutchinson, 1948]

 $\dot{N}(t) = N(t)[1 - N(t - r)]$

Controller Synthesis

Formal Verification

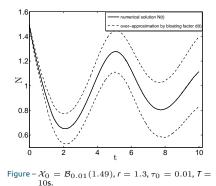
Concluding Remarks

Bounded Verification – Validated Simulation-Based

Example : Delayed Logistic Equation

[G. Hutchinson, 1948]

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Controller Synthesis

Formal Verification

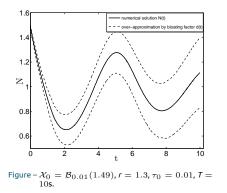
Concluding Remarks

Bounded Verification – Validated Simulation-Based

Example : Delayed Logistic Equation

[G. Hutchinson, 1948]

 $\dot{N}(t) = N(t)[1 - N(t - r)]$



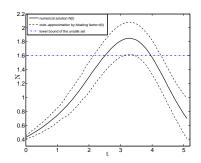


Figure – Over-approximation rigorously proving unsafe, with r = 1.7, $\mathcal{X}_0 = \mathcal{B}_{0.025}(0.425)$, $\tau_0 = 0.1$, T = 5s, $\mathcal{U} = \{N|N > 1.6\}$.

Controller Synthesis

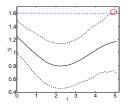
Formal Verification

Concluding Remarks

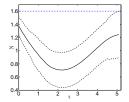
Bounded Verification – Validated Simulation-Based

Example : Delayed Logistic Equation

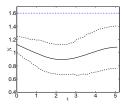
[G. Hutchinson, 1948]



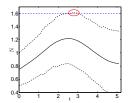
(a) An initial over-approximation of trajectories starting from B_{0.225} (1.25). It overlaps with the unsafe set (s. circle). Initial set is consequently split (cf. Figs. 3b, 3c).



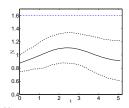
(b) All trajectories starting from B_{0.125}(1.375) are proven safe within the time bound, as the overapproximation does not intersect with the unsafe set.



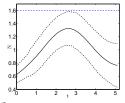
(c) Initial state set B_{0.125}(1.125) is verified to be safe as well.



(d) B_{0.25}(0.75) yields overlap w. unsafe; the ball is partitioned again (Figs. 3e, 3f).



(e) All trajectories originating from B_{0.125} (0.875) are provably safe.



(f) All trajectories originating from B_{0.125}(0.625) are provably safe as well.

Fig. 3: The logistic system is proven safe through 6 rounds of simulation with base stepsize $\tau_0 = 0.1$. Delay r = 1.3, initial state set $\mathcal{X}_0 = \{N | N \in [0.5, 1.5]\}$, time bound T = 5s, unsafe set $\{N | N > 1.6\}$.

Controller Synthesis

Formal Verification

Concluding Remarks

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Bounded Verification – Validated Simulation-Based

Example : Delayed Microbial Growth

[S. F. Ellermeyer, 1994]

$$\begin{cases} \dot{S}(t) = 1 - S(t) - f(S(t))x(t) \\ \dot{x}(t) = e^{-r}f(S(t-r))x(t-r) - x(t) \end{cases}$$

Controller Synthesis

Formal Verification

Concluding Remarks

Bounded Verification – Validated Simulation-Based

Example : Delayed Microbial Growth

[S. F. Ellermeyer, 1994]

$$\begin{cases} \dot{S}(t) = 1 - S(t) - f(S(t))x(t) \\ \dot{x}(t) = e^{-r}f(S(t-r))x(t-r) - x(t) \end{cases}$$

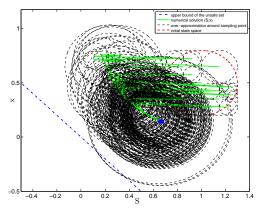
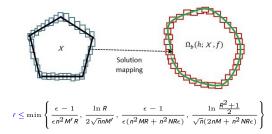


Figure – The microbial system is proven safe by 17 rounds of simulation with $\tau_0 = 0.45$. Here, f(S) = 2eS/(1+S), r = 0.9, $\mathcal{X}_0 = \mathcal{B}_{0.3}((1; 0.5))$, $\mathcal{U} = \{(S; x)|S + x < 0\}$, T = 8s.

Bounded Verification – Boundary Propagation-Based

Boundary Propagation-Based Approximation of Reachable Sets

- Impose a homeomorphism by bounding the time-lag through sensitivity analysis.
- Compute an enclosure of the reachable set's boundary.
- Over- (under-)approximate the reachable set by incl. (excl.) the enclosure.

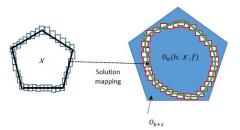


⇒ B. Xue, P. Mosaad, M. Fränzle, M. Chen, Y. Li, N. Zhan : Safe approx. of reachable sets for DDEs. FORMATS '17.

Bounded Verification – Boundary Propagation-Based

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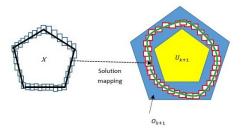


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Bounded Verification – Boundary Propagation-Based

Boundary Propagation-Based Approximation of Reachable Sets

- Impose a homeomorphism by bounding the time-lag through sensitivity analysis.
- Compute an enclosure of the reachable set's boundary.
- **3** Over- (under-)approximate the reachable set by incl. (excl.) the enclosure.



⇒ B. Xue, P. Mosaad, M. Fränzle, M. Chen, Y. Li, N. Zhan : Safe approx. of reachable sets for DDEs. FORMATS '17.

Unbounded Verification

Unbounded Safety Verification of DDEs



Controller Synthesis

Formal Verification

Concluding Remarks

Unbounded Verification – Interval Taylor Enclosure-Based

Unbounded Analysis for Simple DDE $\dot{\mathbf{x}}(t) = \mathbf{f}(\mathbf{x}(t-r))$

Main Ingredients

Generate Taylor series for the segment $x|_{[nr,(n+1)r]}$ by integrating $f(x)|_{[(n-1)r,nr]}$.

- © Degree of Taylor series grows indefinitely (and rapidly so i.g.).
- Computationally intractable.
- S Lacking means for analyzing unbounded behaviors.

⇒ L. Zou, M. Fränzle, N. Zhan, P. N. Mosaad : Automatic stability and safety verification for DDEs. CAV '15.

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2 Overapproximate segments by Interval Taylor Series (ITS) of fixed degree.

- © Tractable (if degree low enough).
- © Thus permits bounded model checking.
- Still no immediate means for unbounded analysis.

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2 Overapproximate segments by Interval Taylor Series (ITS) of fixed degree.

- © Tractable (if degree low enough).
- © Thus permits bounded model checking.
- Still no immediate means for unbounded analysis.
- Extract operator computing next ITS from current one; analyse its properties.
 Unbounded safety and stability analysis become feasible.

⇒ L. Zou, M. Fränzle, N. Zhan, P. N. Mosaad : Automatic stability and safety verification for DDEs. CAV '15.

Controller Synthesis

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Unbounded Verification – Interval Taylor Enclosure-Based

Analysis of a Linear DDE by Example

Recall the DDE $\dot{x}(t) = -x(t-1)$ with the initial condition $x([0,1]) \equiv 1$.

Controller Synthesis

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Unbounded Verification – Interval Taylor Enclosure-Based

Analysis of a Linear DDE by Example

Recall the DDE $\dot{x}(t) = -x(t-1)$ with the initial condition $x([0,1]) \equiv 1$.

Segmentwise integration yields

$$\mathbf{x}(\mathbf{n}+\mathbf{t}) = \mathbf{x}(\mathbf{n}) + \int_{\mathbf{n}-1}^{\mathbf{n}-1+\mathbf{t}} - \mathbf{x}(\mathbf{s}) \, \mathrm{d}\mathbf{s}, \quad \mathbf{t} \in [0,1].$$

Controller Synthesis

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Unbounded Verification – Interval Taylor Enclosure-Based

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■ Rename and shift $x|_{[n,n+1]}$, with $n \in \mathbb{N}$, to $f_n \colon [0,1] \mapsto \mathbb{R}$ by setting $f_n(t) \cong x(n+t)$ for $t \in [0,1]$:

$$f_n(t) = f_{n-1}(1) + \int_0^t -f_{n-1}(s) \,\mathrm{d}s, \quad t \in [0,1].$$

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$$f_n(t) = f_{n-1}(1) + \int_0^t -f_{n-1}(s) \,\mathrm{d}s, \quad t \in [0,1].$$

- \bigcirc f_n is a polynomial of degree n, i.e., degree 86,400 after a day, ...
- Intractable beyond the first few steps!

Controller Synthesis

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Concluding Remarks

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Unbounded Verification – Interval Taylor Enclosure-Based

Analysis of a Linear DDE by Example

- Employ interval Taylor series to enclose the segmentwise solutions by Taylor series of fixed degree
 - Fixing degree 2, e.g., yields template $f_n(t) = a_{n_0} + a_{n_1} * t + a_{n_2} * t^2$,
 - interval coefficients *a_{ni}* incorporate the approximation error.

Controller Synthesis

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Unbounded Verification – Interval Taylor Enclosure-Based

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 - Fixing degree 2, e.g., yields template $f_n(t) = a_{n_0} + a_{n_1} * t + a_{n_2} * t^2$,
 - interval coefficients *a_{ni}* incorporate the approximation error.
- For computing the ITS, we need to obtain the first and second derivatives $f_{n+1}^{(1)}(t)$ and $f_{n+1}^{(2)}(t)$ based on f_n :

$$\begin{split} f_{n+1}^{(1)}(t) &= -f_n(t) = -a_{n0} - a_{n1} * t - a_{n2} * t^2, \\ f_{n+1}^{(2)}(t) &= \frac{\mathrm{d}}{\mathrm{d}t} f_{n+1}^{(1)}(t) = -a_{n1} - 2 * a_{n2} * t. \end{split}$$

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Unbounded Verification – Interval Taylor Enclosure-Based

Analysis of a Linear DDE by Example

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• Using a Lagrange remainder with fresh variable $\eta_n \in [0, 1]$, we obtain

$$\begin{aligned} f_{n+1}(t) &= f_n(1) + \frac{f_n^{(1)}(0)}{1!} * t + \frac{f_n^{(2)}(\eta_n)}{2!} * t^2 \\ &= (a_{n0} + a_{n1} + a_{n2}) - a_{n0} * t - \frac{a_{n1} + 2 * a_{n2} * \eta_n}{2} * t^2 \end{aligned}$$

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Unbounded Verification – Interval Taylor Enclosure-Based

Analysis of a Linear DDE by Example

Substituting $f_{n+1}(t)$ by its Taylor form $a_{n+1_0} + a_{n+1_1} * t + a_{n+1_2} * t^2$ and matching coefficients, one obtains a time-variant, parametric linear operator

$$\begin{bmatrix} a_{n+1_0} \\ a_{n+1_1} \\ a_{n+1_2} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ -1 & 0 & 0 \\ 0 & -\frac{1}{2} & -\eta_n \end{bmatrix} * \begin{bmatrix} a_{n_0} \\ a_{n_1} \\ a_{n_2} \end{bmatrix}$$

which can be made time-invariant by replacing η_n with its interval [0, 1].

 $\odot\,$ Have thus obtained a $\mbox{discrete-time}$ interval-linear system $\mathbf{a}'=\mathcal{M}\mathbf{a}!$

Formal Verification

Concluding Remarks

Unbounded Verification – Interval Taylor Enclosure-Based

Stability of Linear DDEs

Observation : The global solution x to the DDE stabilizes asymptotically if the sequence of segments f_n converges to 0, iff the coefficients A_n of the interval Taylor forms converge to 0.

Controller Synthesis

Formal Verification

Concluding Remarks

Unbounded Verification – Interval Taylor Enclosure-Based

Stability of Linear DDEs

Observation : The global solution x to the DDE stabilizes asymptoticallyif the sequence of segments f_n converges to 0,iff the coefficients A_n of the interval Taylor forms converge to 0.

 $\label{eq:consequence: Consequence: Conseq$

Theorem (J. Daafouz and J. Bernussou, 2001)

The time-variant system $\mathbf{x}(n + 1) = T(\boldsymbol{\eta}(n)) * \mathbf{x}(n)$, $T(\boldsymbol{\eta}(n)) = \sum_{i=1}^{q} \eta_i(n) * T_i$, with $\eta_i(n) \ge 0$, $\sum_{i=1}^{q} \eta_i(n) = 1$, is asymptotically/robustly stable iff there exist symmetric positive definite matrices S_i , S_j and matrices G_i of appropriate dimensions s.t.

$$\begin{bmatrix} G_i + G_i^{\mathsf{T}} & G_i^{\mathsf{T}} & T_i^{\mathsf{T}} \\ T_i & G_i & S_j \end{bmatrix} > 0$$

for all i = 1, ..., N and j = 1, ..., N. Moreover, the corresponding Lyapunov function is

$$V(\mathbf{x}(n), \boldsymbol{\eta}(n)) = \mathbf{x}(n)^{\mathsf{T}} * (\sum_{i=1}^{q} \boldsymbol{\eta}_{i}(n) * S_{i}^{-1}) * \mathbf{x}(n).$$

Just requires some technicalities to obtain appropriate interval forms for applicability of Rohn's method for solving linear interval inequalities.

Formal Verification

Concluding Remarks

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Unbounded Verification – Interval Taylor Enclosure-Based

Unbounded Safety Verification for Linear DDEs

 $\ensuremath{{}^{\odot}}$ Verifying **unbounded safety** $\Box \mathcal{S}$ can be accomplished by

- **1** generating a Lyapunov function $V(\mathbf{A}, \eta)$ by above method,
- **2** computing a barrier value for the safe set by letting iSAT search for the largest *c* such that $V(\mathbf{A}(n), \eta(n)) \leq c \land \neg S(f_n(t))$ is unsatisfiable,
- ⇒ existence of such *c* implies that $V(\mathbf{A}(n), \eta_n) \leq c \rightarrow S(f_n(t))$ holds.

Unbounded Verification – Interval Taylor Enclosure-Based

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- **i** calculating a safe bound on the minimum reduction d_m on the condition $V(\mathbf{A}(n), \eta(n)) \ge c$, i.e.

 $d_{m} = \min\{V(\mathbf{A}(n), \eta(n)) - V(\mathbf{A}(n+1), \eta_{n+1}) \mid V(\mathbf{A}(n), \eta_{n}) \ge c\},\$

by iSAT optimization.

⇒ Existence of such d_m implies that after $k \cong \max\left(\frac{V(A(0), 0) - c}{d_m}, \frac{V(A(0), 1) - c}{d_m}\right)$ we can be sure to reside inside the safety region S.

Unbounded Verification – Interval Taylor Enclosure-Based

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- 4 Pursuing BMC for the first *k* steps, which completes proving unbounded invariance.

Controller Synthesis

Formal Verification

Concluding Remarks

Unbounded Verification – Interval Taylor Enclosure-Based

Multidimensional Polynomial DDEs

Consider a DDE of the form

 $\dot{\mathbf{x}}(t+t) = \boldsymbol{g}(\mathbf{x}(t)), \ \forall t \in [0, t] \colon \mathbf{x}(t) = \mathbf{p}_0(t),$

where \boldsymbol{g} and $\mathbf{p}_0(t)$ are vectors of polynomials in $\mathbb{R}^m[\mathbf{x}]$.

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Unbounded Verification – Interval Taylor Enclosure-Based

Multidimensional Polynomial DDEs

Consider a DDE of the form

$$\dot{\mathbf{x}}(\boldsymbol{t}+\boldsymbol{r}) = \boldsymbol{g}(\mathbf{x}(\boldsymbol{t})), \,\forall \boldsymbol{t} \in [0, \boldsymbol{r}] \colon \mathbf{x}(\boldsymbol{t}) = \mathbf{p}_0(\boldsymbol{t}),$$

where \boldsymbol{g} and $\mathbf{p}_0(t)$ are vectors of polynomials in $\mathbb{R}^m[\mathbf{x}]$.

■ Generalizing the linear case, the Lie derivatives $f_{n+1}^{(1)}, f_{n+1}^{(2)}, \ldots, f_{n+1}^{(k)}$ can now be computed *symbolically* as follows :

$$\boldsymbol{f}_{n+1}^{(1)}(t) = \boldsymbol{g}(\boldsymbol{f}_n(t)), \quad \boldsymbol{f}_{n+1}^{(2)}(t) = \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{f}_{n+1}^{(1)} = \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{g}(\boldsymbol{f}_n(t)), \dots$$

The corresponding Taylor expansion of $f_{n+1}(t)$ with degree k is

$$\boldsymbol{f}_{n+1}(t) = \boldsymbol{f}_n(t) + \frac{\boldsymbol{f}_{n+1}^{(1)}(0)}{1!} * t + \dots + \frac{\boldsymbol{f}_{n+1}^{(k-1)}(0)}{(k-1)!} * t^i + \frac{\boldsymbol{f}_{n+1}^{(k)}(\boldsymbol{\eta}_n)}{k!} * t^k,$$

where η_n is a vector ranging over $[0, r]^m$.

Controller Synthesis

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Unbounded Verification – Interval Taylor Enclosure-Based

Multidimensional Polynomial DDEs

Akin to the linear case, the above equation can be rephrased as a time-invariant polynomial interval operator

$$\mathbf{A}(\mathbf{n}+1) = \mathbf{P}(\mathbf{A}(\mathbf{n}), [0, \mathbf{r}]), \tag{(\dagger)}$$

where P this time is a vector of polynomials.

Formal Verification

Concluding Remarks

Unbounded Verification – Interval Taylor Enclosure-Based

Multidimensional Polynomial DDEs

Akin to the linear case, the above equation can be rephrased as a time-invariant polynomial interval operator

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where P this time is a vector of polynomials.

- S Apply polynomial constraint solving to
 - pursue BMC exactly as before, unwinding relation (†),
 - find a relaxed Lyapunov function by instantiating a polynomial Lyapunov function template w.r.t. (†), using the method in [S. Ratschan and Z. She, SIAM J. of Control and Optimiz., 2010],
 - compute barrier values for a safe set,
 - ...

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Unbounded Verification – Linearization & Spectral Analysis-Based

Stability of General Linear Dynamics by Spectral Analysis

For linear DDEs :

 $\dot{\mathbf{x}}(t) = A\mathbf{x}(t) + B\mathbf{x}(t-r)$

Controller Synthesis

Formal Verification

Concluding Remarks

Unbounded Verification – Linearization & Spectral Analysis-Based

Stability of General Linear Dynamics by Spectral Analysis

For linear DDEs :

$$\dot{\mathbf{x}}(t) = A\mathbf{x}(t) + B\mathbf{x}(t-t)$$

$$\det\left(\lambda I - A - B \mathrm{e}^{-r\lambda}\right) = 0$$

Controller Synthesis

Formal Verification

Concluding Remarks

Unbounded Verification – Linearization & Spectral Analysis-Based

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Controller Synthesis

Formal Verification

Concluding Remarks

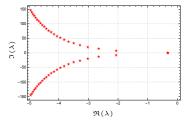
Unbounded Verification – Linearization & Spectral Analysis-Based

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Controller Synthesis

Formal Verification

Concluding Remarks

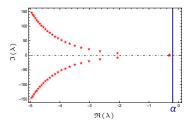
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Stability of General Linear Dynamics by Spectral Analysis

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Controller Synthesis

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Unbounded Verification - Linearization & Spectral Analysis-Based

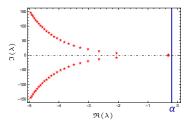
Stability of General Linear Dynamics by Spectral Analysis

For linear DDEs :

 $\dot{\mathbf{x}}(t) = A\mathbf{x}(t) + B\mathbf{x}(t - r)$

The characteristic equation :

$$\det\left(\lambda I - \mathbf{A} - \mathbf{B} \mathrm{e}^{-\mathbf{r}\lambda}\right) = 0$$



Globally exponentially stable if $\forall \lambda \colon \mathfrak{R}(\lambda) < 0$, i.e.,

 $\exists \mathbf{K} > 0. \ \exists \alpha < 0: \ \left\| \mathbf{\xi}_{\boldsymbol{\phi}}(t) \right\| \leq \mathbf{K} \| \boldsymbol{\phi} \| e^{\alpha t}, \quad \forall t \geq 0, \ \forall \boldsymbol{\phi} \in \mathcal{C}_{\mathbf{F}}$

Controller Synthesis

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Concluding Remarks

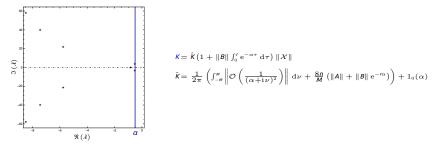
Unbounded Verification – Linearization & Spectral Analysis-Based

Reduction to Bounded Verification

[PD-Controller, E. Goubault et al., CAV '18]

1 Identify the rightmost eigenvalue (and hence α) and construct *K*.

2 Compute T* based on the exponential estimation spanned by α and K.
 3 Reduce to bounded verifi., i.e., ∀T > T*, ∞-safe ↔ T-safe.



Controller Synthesis

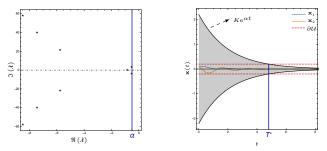
 Concluding Remarks

Unbounded Verification - Linearization & Spectral Analysis-Based

Reduction to Bounded Verification

[PD-Controller, E. Goubault et al., CAV '18]

- **I** Identify the rightmost eigenvalue (and hence α) and construct *K*.
- **Z** Compute T^* based on the exponential estimation spanned by α and K.
- **B** Reduce to bounded verifi., i.e., $\forall T > T^*$, ∞ -safe \iff *T*-safe.



Controller Synthesis

Formal Verification

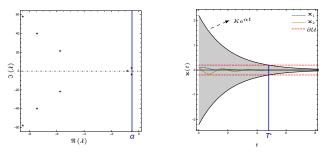
Concluding Remarks

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Controller Synthesis

Formal Verification

Concluding Remarks

Unbounded Verification – Linearization & Spectral Analysis-Based

Stability of General Nonlinear Dynamics by Linearization

For nonlinear DDEs :

$$\dot{\mathbf{x}}(t) = \boldsymbol{f}(\mathbf{x}(t), \mathbf{x}(t-t))$$

= $A\mathbf{x} + B\mathbf{y} + \boldsymbol{g}(\mathbf{x}, \mathbf{y})$, with $A = \boldsymbol{f}_{\mathbf{x}}(0, 0), B = \boldsymbol{f}_{\mathbf{y}}(0, 0)$

Controller Synthesis

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Unbounded Verification – Linearization & Spectral Analysis-Based

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The linearization yields

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Unbounded Verification - Linearization & Spectral Analysis-Based

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The linearization yields

$$\dot{\mathbf{x}}(t) = A\mathbf{x}(t) + B\mathbf{x}(t-r)$$

Locally exponentially stable if $\forall \lambda \colon \Re(\lambda) < 0$, i.e.,

 $\exists \delta > 0, \exists \mathbf{K} > 0, \exists \alpha < 0; \| \boldsymbol{\phi} \| \leq \delta \implies \| \boldsymbol{\xi}_{\boldsymbol{\phi}}(t) \| \leq \mathbf{K} \| \boldsymbol{\phi} \| e^{\alpha t/2}, \quad \forall t \geq 0$

Controller Synthesis

 Concluding Remarks

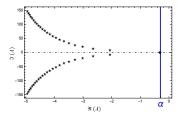
Unbounded Verification - Linearization & Spectral Analysis-Based

Reduction to Bounded Verification

[Population Dynamics, G. Hutchinson, 1948]

Identify the rightmost eigenvalue (and hence α), then construct K and δ .

- **2** Compute T^* , as well as T' (by bounded verifiers) s.t. $\|\Omega\| < \delta$ within T'.
- **3** Reduce to bounded verifi., i.e., $orall T > T' + T^*$, ∞ -safe \iff T-safe.



$$\begin{split} \delta &= \min\left\{\delta_{\epsilon}, \delta_{\epsilon} / \left(\hat{k} \mathrm{e}^{-r\alpha} \left(1 + \|\boldsymbol{B}\| \int_{0}^{t} \mathrm{e}^{-\alpha\tau} \, \mathrm{d}\tau\right)\right)\right\}\\ \delta_{\epsilon} &= \hat{k} \mathrm{e}^{-r\alpha} \left(1 + \|\boldsymbol{B}\| \int_{0}^{t} \mathrm{e}^{-\alpha\tau} \, \mathrm{d}\tau\right) \|\boldsymbol{\phi}\| \, \mathrm{e}^{\epsilon \hat{K} \mathrm{e}^{-r\alpha} t + \alpha t}\\ \epsilon &\leq -\alpha / (2 \hat{k} \mathrm{e}^{-r\alpha}) \end{split}$$

Controller Synthesis

 Concluding Remarks

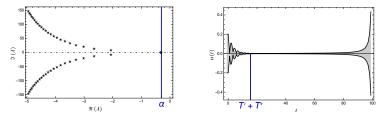
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Controller Synthesis

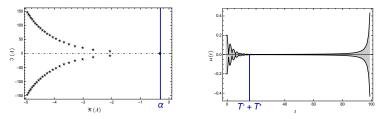
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Reduction to Bounded Verification

[Population Dynamics, G. Hutchinson, 1948]

- **1** Identify the rightmost eigenvalue (and hence α), then construct K and δ .
- **Z** Compute T^* , as well as T' (by bounded verifiers) s.t. $\|\Omega\| < \delta$ within T'.
- **3** Reduce to bounded verifi., i.e., $\forall T > T' + T^*$, ∞ -safe \iff *T*-safe.



Controller Synthesis

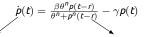
Formal Verification

Concluding Remarks

Unbounded Verification – Linearization & Spectral Analysis-Based

Non-Polynomial Dynamics : Disease Pathology

[M. C. Mackey and L. Glass, 1977]



#mature blood cells in circulation delay btw. cell production and maturation

Controller Synthesis

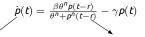
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Parameters : $\theta = n = 1, \beta = 0.5, \gamma = 0.6, r = 0.5$.

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Controller Synthesis

Formal Verification

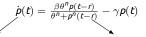
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Linearization yields

 $\dot{\mathbf{p}}(t) = -0.6\mathbf{p}(t) + 0.5\mathbf{p}(t - 0.5).$

Critical values : $\alpha = -0.07$, K = 1.75081, $\delta = 0.0163426$, $T^* = 0$.

Controller Synthesis

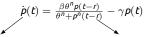
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By bounded verification [E. Goubault et al., CAV '18], with Taylor models of the order 5 :

 $\left\| \left. \Omega \right|_{[25,45,25,95]} \right\| < \delta \quad \text{and} \quad \Omega \left|_{[-0.5,25,95+0]} \cap \mathcal{U} = \emptyset.$

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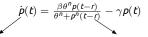
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↓ ∞-safetv

Unbounded Verification - Linearization & Spectral Analysis-Based

Comparison with Existing Methods for Unbounded Verification

- Allow immediate feedback, i.e, x(t), as well as multiple delays in the dynamics, to which the technique in [L. Zou et al., CAV'15] does not generalize immediately.
- © No polynomial template needs to be specified, yet necessarily for the *interval Taylor models* in [L. Zou et al., CAV'15] and [P. N. Mosaad et al., ICTAC'16], for Lyapunov functionals in [M. Peet and S. Lall, NOLCOS'04], or for barrier certificates in [S. Prajna and A. Jadbabaie, CDC'05].
- © Delay-dependent stability certificate, other than the *absolute stability* exploited in [M. Peet and S. Lall, NOLCOS'04], i.e., a criterion requiring stability for arbitrarily large delays.
- Confined to differential dynamics featuring exponential stability. Investigation of more permissive forms of stability, e.g., asymptotical stability, that may admit a similar reduction-based idea, is subject to future work.

Outline

1 Synthesizing Safe Controllers Resilient to Delayed Interaction

- Safety Games under Delays
- Incremental Synthesis
- Equivalent Controllability

2 Verifying Safety of Delayed Differential Dynamics

- Delayed Differential Dynamics
- Bounded Safety Verification
- Unbounded Safety Verification

3 Concluding Remarks

Summary

Motivation	Controller Synthesis	Formal Verification	Concluding Remarks
			$\circ \bullet \circ$
Summary			

Concluding Remarks

Problem : We face

- increasingly wide-spread use of networked distributed sensing and control,
- substantial feedback delays thus affecting hybrid control schemes,
- delays impact controllability and control performance in both the discrete and the continuous parts.

Status: We present

- safety games under delays and incremental algorithm for efficient control synthesis,
- bounded safety verification methods for delayed differential dynamics,
- extension to unbounded verification by leveraging stability criteria.

Future Work : We'd explore

- controller synthesis for delayed hybrid systems in the setting of continuous time,
- DDE exhibiting state-dependent or/and stochastic delay,
- hybrid automata comprising DDEs instead of ODEs,
- hybrid automata combining delayed continuous & discrete reactive behaviors,
- invariant generation for time-delayed systems.



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