Compiler Construction

Lecture 19: Code Generation V (Machine Code)

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(Software Modeling and Verification)

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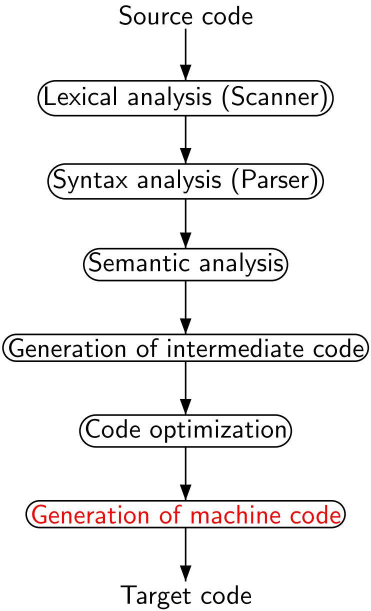
Summer Semester 2014

Outline

1. Generation of Machine Code
2. Register Allocation
3. Outlook

Conceptual Structure of a Compiler



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Final step: translation of (optimized) abstract machine code into "real" machine code (possibly followed by assembling phase)

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- main memory ("slow" RAM)
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Instruction set: depending on

- number of operands
- type of operands
- addressing modes

Code Generation Phases

1. Register allocation: registers used for
   - values of (frequently used) variables and intermediate results
   - computing memory addresses (array indexing, ...)
   - passing parameters to procedures/functions
2. Instruction selection:
   - translation of abstract instructions into (sequences of) real instructions
   - employ special instructions for efficiency
     (e.g., `INC(x)` rather than `ADD(x,1)`)
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and main memory `M`

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Instruction types:

$\mathtt{R}_i$:= $\mathtt{M}[a]$
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- **Idea:** start with register-intensive subexpressions

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  - if $r_2 < r_1 \leq r$, then e can be evaluated using r_1 registers
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- The corresponding optimization algorithm works in two phases:
  1. Marking phase (computes r_i values)
  2. Generation phase (produces actual code)

  (for details see Wilhelm/Maurer: *Übersetzerbau, 2. Auflage*, Springer, 1997, Sct. 12.4)

The Marking Phase

Algorithm 19.2 (Marking phase)

Input: *expression (with binary operators op and variables x)*

Procedure: *recursively compute*

$$r(x) := \begin{cases} 1 & \text{if } x \text{ is a ``left leaf''} \\ 0 & \text{if } x \text{ is a ``right leaf''} \\ 1 & \text{if } x \text{ is at the root} \end{cases}$$

$$r(e_1 \ op \ e_2) := \begin{cases} \max\{r(e_1), r(e_2)\} & \text{if } r(e_1) \neq r(e_2) \\ r(e_1) + 1 & \text{if } r(e_1) = r(e_2) \end{cases}$$

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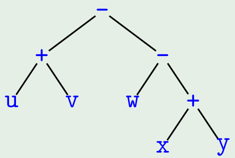

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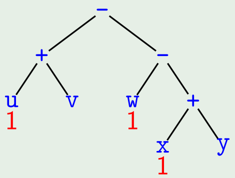

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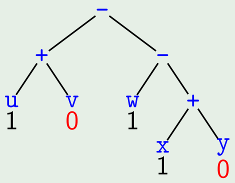

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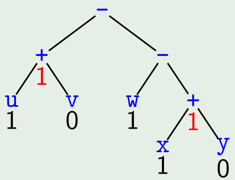

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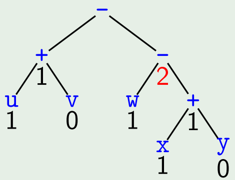

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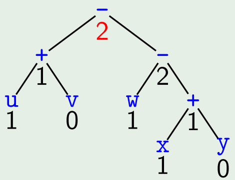

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- Data structures used in Algorithm 19.4:

  RS: stack of available registers (initially: all registers; never empty)

  CS: stack of available main memory cells
- Auxiliary procedures used in Algorithm 19.4:

  output: outputs the argument as code

  top: returns the topmost entry of a stack S (leaving S unchanged)

  pop: removes and returns the topmost entry of a stack

  push: puts an element onto a stack

  exchange: exchanges the two topmost elements of a stack

Algorithm 19.4 (Generation phase)

Input: *expression e, annotated with register requirement $r(e)$*

Variables: *RS: stack of registers;*
CS: stack of memory cells;
R: register; C: memory cell;

Procedure: *recursive execution of procedure $code(e)$, defined by $code(e) :=$*

(1) if $e = x$, $r(x) = 1$: % left leaf
  $output(top(RS)\texttt{:=}\ \texttt{M[}x\texttt{]})$

(2) if $e = e_1$ op y, $r(y) = 0$: % right leaf
  $code(e_1)$;
  $output(top(RS)\texttt{:=}top(RS)\ op\ \texttt{M[}y\texttt{]})$

(3) if $e = e_1$ op e_2, $r(e_1) < r(e_2)$, $r(e_1) < r$:
  $exchange(RS)$;
  $code(e_2)$;
  $R := pop(RS)$;
  $code(e_1)$;
  $output(top(RS)\texttt{:=}top(RS)\ op\ R)$;
  $push(RS, R)$;
  $exchange(RS)$

(4) if $e = e_1$ op e_2, $r(e_1) \geq r(e_2)$, $r(e_2) < r$:
  $code(e_1)$;
  $R := pop(RS)$;
  $code(e_2)$;
  $output(R\texttt{:=}R\ op\ top(RS))$;
  $push(RS, R)$

(5) if $e = e_1$ op e_2, $r(e_1) \geq r$, $r(e_2) \geq r$:
  $code(e_2)$;
  $C := pop(CS)$;
  $output(\texttt{M[}C\texttt{]:=}top(RS))$;
  $code(e_1)$;
  $output(top(RS)\texttt{:=}top(RS)\ op\ \texttt{M[}C\texttt{]})$;
  $push(CS, C)$

Output: *optimal (= shortest) code for evaluating e*

The Generation Phase III

- Invariants of Algorithm 19.4:
  - after executing *code*(e), both *RS* and *CS* have their original values
  - after executing the machine code produced by *code*(e), the value of e is stored in the topmost register of *RS*

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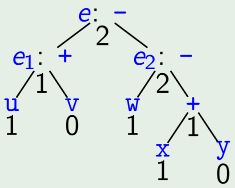

(on the board)

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1. Use unbounded number of symbolic registers for storing intermediate values
2. Consider life span of symbolic registers: r is live at program point p if
   - there is a path to p on which r is set and
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6. Program executable with k real registers iff collision graph k-colorable

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Further Topics in Compiler Construction

- Translation of higher-level constructs (modules, classes, ...)
- Translation of non-procedural languages
  - object-oriented (polymorphism, dynamic dispatch)
  - functional (higher-order functions, type checking/inference)
  - logic (unification, backtracking)
- Code optimization
- Symbol-table handling
- Error handling
- Bootstrapping

Exams & Seminar

Exams

1. Friday, 25 July, 10:00–13:00, AH 1 (BSc), AH 4 (MSc)
2. Wednesday, 3 September, 10:00–13:00, AH 4

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Winter Semester 2014/15: Trends in Computer-Aided Verification

- Axiomatic Verification [C. Jansen]
- Graph-Based Abstraction [T. Noll]
- Inductive Incremental Verification [T. Lange]
- Verification of Probabilistic Systems [K. van der Pol]
- Companion seminar: Probabilistic Programs
  [J.-P. Katoen, N. Jansen, B. Kaminski, F. Olmedo]

Lectures

Winter Semester 2014/15: Static Program Analysis

- Dataflow analysis
- Abstract interpretation
- Interprocedural analysis
- Pointer analysis

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Summer Semester 2015: Semantics and Verification of Software

- Operational semantics
- Denotational semantics
- Axiomatic semantics
- Semantic equivalence
- Compiler correctness